Remarks

Applicants appreciate the Examiner's indication that claim 12 is allowable and that claim 7 is directed to allowable subject matter. Additionally, in the Office Action of June 3, 2005, the Examiner rejected claims 14-19 under 35 U.S.C. § 103(a) as being unpatentable in view of U.S. Patent No. 5,517,671 to Parks et al. ("Parks"), in view of U.S. Patent No. 6,065,088 to Bronson et al. ("Bronson") and U.S. Patent No. 5,928,354 to Umeki et al. ("Umeki"); and rejected claims 1, 2, 5, 6, 8, 9, 13, and 20-25 under 35 U.S.C. § 103(a) over Bronson in view of Umeki.

By this Amendment, Applicants have amended claims 1, 2, 5, 7, 8, 12, 13, and 20 to improve form and added new claims 26 and 27. Support for new claims 26 and 27 can be found at, for example, paragraphs 51 and 52 of the originally filed specification.

Rejection of Claims 1, 2, 5, 6, 8, 9, 13, and 20-25 *Based on Bronson and Umeki*

Claim 1, as amended, includes a first queue, a second queue, and bypass logic. The first queue is configured to enqueue and dequeue data units and includes a plurality of parallel sub-queues that queue a plurality of parallel data units. The second queue is configured to receive data units from the first queue when the first queue has data units available to be dequeued. The second queue includes a first buffer configured to store a first set of the parallel data units and a second buffer configured to store a second set of the parallel data units. The bypass logic is coupled to the second queue. The bypass logic is

configured to bypass the first queue and to forward data units to the second queue when the second queue is ready to receive data units and the first queue is empty.

Applicants submit that Bronson and Umeki, either alone or in combination, fail to disclose or suggest each of the elements recited in claim 1. These references, for instance, fail to disclose or suggest the first and second queues recited in claim 1.

As discussed in the previous Amedment, Bronson is directed to systems and methods for interrupt command queuing and ordering. (Bronson, Title). The Examiner contends that interrupt routing unit 142 of Bronson (see Bronson, Fig. 3) corresponds to the first queuing area (now recited as the first queue) and the remaining queues correspond to the claimed second queuing area (now recited as the second queue). (Office Action, page 6). Applicants disagree.

Interrupt routing unit 142 of Bronson handles interrupt commands and is particularly discussed by Bronson at column 8, lines 20-54. As disclosed by Bronson, interrupt routing unit 142 has two separate command queues, queue 136 for EOI (end-of-interrupt) commands and queue 134 for both INR (interrupt return) and IRR (interrupt reissue request) commands. (Bronson, col. 8, lines 20-23). The EOI commands output from queue 136 are fed into queue 146, which, according to Bronson, is "implemented as a strict First In First Out (FIFO) queue." (Bronson, col. 8, lines 33-36). The INR and IRR commands output from queue 134, on the other hand, are delivered to high priority I/O command queue 150. (Bronson, col. 8, lines 42-45).

Bronson cannot be said to include, as recited in claim 1, a first queue configured to enqueue and dequeue data units, the first queue including a plurality of parallel sub-queues that queue a plurality of parallel data units. The Examiner contends that EOI output queue 136 and INR/IRR output queue 134 of Bronson correspond to the plurality of sub-queues recited in claim 1. (Office Action, page 6). Applicants respectfully disagree with the Examiner's interpretation of Bronson. Although queues 136 and 134 of Bronson define multiple queues, these queues appear to each be separate queues that are used to queue different commands and that output the commands to different output queues. Accordingly, it is not accurate to interpret these queues as a first queue that includes a "plurality of sub-queues" that queue "a plurality of parallel data units," as recited in claim 1. Queues 136 and 134 are not sub-queues of a larger queue, they are independent queues that are part of an interrupt routing unit 142.

Bronson cannot be said to include, as is further recited in claim 1, a second queue that includes a first buffer configured to store a first set of parallel data units and a second buffer configured to store a second set of the parallel data units. The Examiner contends that this feature is disclosed by priority queues 148 and 150 of Bronson. (Office Action, page 6). Applicants submit that queues 148 and 150 of Bronson are not buffers that store first and second sets of parallel data units. Queues 148 and 150 are described by Bronson as a "normal priority queue" that receives commands from command queue 146 and a "high priority queue" that receives commands from output queue 134. Because these queues correspond to different priority data and receive different types of

commands from different sources, it is not accurate to say that these queues correspond to first and second buffers of a single queue that store first and second sets of parallel data. Queues 148 and 150 are two independent queues, not buffers of a single queue. Additionally, queues 148 and 150 do not store sets of parallel data units, instead, the data in queues 148 and 150 appear to progress through queues 148 and 150 in a non-parallel manner in which queue 150 is given higher priority.

Arguments similar to those in the previous two paragraphs were presented in the previous Amendment. In response, the Examiner contends that the previously recited "queuing areas" can be interpreted to encompass multiple different queues, such as queues 148 and 150 of Bronson. (Office Action, page 2). Although Applicants do not agree with the Examiner's interpretation of the phrase "queuing area," Applicants note that claim 1, as amended, now recites first and second queues. For the reasons given above, Bronson does not disclose or suggest a first queue and a second queue as recited in amended claim 1. Instead, as is clearly shown in Fig. 3 and correspondingly described by Bronson, Bronson discloses multiple different queues 134, 146, 146, 148, and 150 that each function as an independent queue.

Umeki does not cure the above-mentioned deficiencies of Bronson. Accordingly, Bronson and Umeki, either alone or in combination, do not disclose all of the features recited in claim 1.

Claim 1 further recites bypass logic coupled to the second queue, where the bypass logic is configured to bypass the first queue and to forward data units

to the second queue when the second queue is ready to receive data units and the first queue is empty. The Examiner concedes that Bronson does not disclose this bypass logic, but contends that Umeki discloses the recited bypass logic and that one of ordinary skill in the art would have found it obvious to combine Bronson and Umeki to obtain the features recited in claim 1. (Office Action, page 6). Applicants respectfully disagree.

Applicants submit that the Examiner has not made a proper *prima facie* case of obviousness, as one of ordinary skill in the art would not combine Bronson and Umeki as the Examiner suggests. More particularly, the Examiner states that "[i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to bypass the first queuing area of Bronson et al. as done by Umeki et al. since doing so improves access reliability and speed." (Office Action, page 6). Umeki discloses skipping an instruction queue buffer 2 leading to a CPU 4. Applicants submit that an instruction queue buffer leading to a CPU is not reasonably related to an interrupt routing unit, such as unit 142 of Bronson. Accordingly, one of ordinary skill in the art reading Umeki would not be motivated to bypass interrupt routing unit 142 of Bronson in the manner suggested by the Examiner.

For at least these reasons, Applicants submit that the rejection of claim 1 under 35 U.S.C. § 103(a) is improper and should be withdrawn. The rejections of claims 2, 5, and 6, at least by virtue of their dependency from claim 1, are also improper and should be withdrawn.

Claims 8, 9, and 13 also stand rejected under 35 U.S.C. § 103(a) based on Bronson and Umeki. Applicants respectfully traverse this rejection.

Claim 8, as amended, is directed to a method of masking latency in a device. The method includes receiving incoming data items that include a plurality of data items that are input to a queue for each cycle of the queue. The method further includes forwarding the incoming data items to a buffer when the queue is empty and the buffer is free to receive data items, wherein the buffer includes a first buffer and a second buffer, and wherein higher priority data items are stored in the first buffer and lower priority data items are stored in the second buffer. The method further includes enqueuing the incoming data items in the queue when the queue contains data items or the buffer is not free to receive data items, dequeuing data items from the queue to the buffer when the buffer is free to receive data items, and transmitting the data items from the buffer as the output of the device.

Bronson and Umeki do not disclose or suggest the combination of features recited in amended claim 8. The Examiner contends that Bronson discloses many of the features recited in claim 8 but concedes that Bronson does not disclose forwarding data items to a buffer when a queue is empty. For this, the Examiner relies on Umeki. (Office Action, page 7).

Applicants submit that Bronson and Umeki, alone or in combination, do not disclose or suggest all of the features recited in claim 8. Bronson, for instance, does not disclose or suggest receiving incoming data items for a queue that includes a plurality of data items that are input to the queue for each cycle of

the queue, as recited in claim 8. The Examiner contends that queue 146 of Bronson corresponds to this queue. (Office Action, page 7). Queue 146, however, is not disclosed as receiving a plurality of data items that are input to the queue for each cycle of the queue. Instead, Bronson explicitly discloses using a multiplexer 144 at the input of queue 146 to select between the MMIO commands and the EOI commands. Accordingly, it appears to Applicants that multiplexer 144, if anything, actually teaches away from receiving a plurality of data items for each cycle of the queue, as recited in claim 8. Further, queue 146 of Bronson is graphically illustrated as a linear array of single slots, which further tends to show that queue 146 of Bronson is not capable of receiving "a plurality of data items for each cycle of the queue," as recited in claim 8.

An argument similar to that made in the previous paragraph was also made in the previously filed Amendment. In response to this argument, the Examiner contends that because multiplexer 144 of Bronson receives multiple commands but only selects one for input to queue 146, "multiple data items are received for each cycle of the queue." (Office Action, page 3). Although Applicants do not necessarily agree with the Examiner's interpretation of claim 8, Applicants submit that claim 8, as amended, clearly recites that the plurality of incoming data items are input to the queue in a cycle of the queue. Accordingly, the multiplexer 144 of Bronson, which the Examiner concedes only transmits a single command to queue 146 each cycle, does not disclose or suggest this feature of claim 8.

Further, Applicants submit that the Examiner has not made a *prima facie* case of for combining Bronson and Umeki as the Examiner suggests. Umeki discloses skipping an instruction queue buffer 2 leading to a CPU 4. An instruction queue buffer leading to a CPU is not reasonably related to the input/output bus bridge and command queuing system of Bronson. Accordingly, one of ordinary skill in the art reading Umeki would not be motivated to modify Bronson in the manner suggested by the Examiner.

For at least these reasons, Applicants submit that Bronson and Umeki, either alone or in combination, do not disclose or suggest each of the features recited in claim 8. Accordingly, the rejection of this claim is improper and should be withdrawn.

Claims 9 and 13, which depend from claim 8, were additionally rejected under 35 U.S.C. § 103(a) in view of Bronson and Umeki. At least by virtue of their dependency from claim 8, Applicants submit that the rejections of these claims are improper and should be withdrawn.

Independent claim 20 was also rejected by the Examiner under 35 U.S.C. § 103(a) in view of Bronson and Umeki. This claim, as amended, includes features similar to those recited in claim 8. Accordingly, for reasons similar to those given above with regard to claim 8, Applicants submit that the rejection of claim 20 under 35 U.S.C. § 103(a) is also improper and should be withdrawn. Additionally, at least by virtue of its dependency from claim 20, Applicants submit that the rejection of claim 21 is also improper and should be withdrawn.

Independent claim 22 and its dependent claims 23-25 also stand rejected under 35 U.S.C. § 103(a) based on Bronson and Umeki. Applicants respectfully traverse this rejection.

Claim 22 is directed to an arbiter comprising a queue, a multiplexer, and arbitration logic. The queue is configured to enqueue data items at a first stage of a plurality of stages and dequeue the data items at a last stage of the plurality of stages of the queue. The multiplexer has a plurality of inputs connected to different stages of the queue. The multiplexer outputs selected ones of the data items read from the queue. The arbitration logic is coupled to the queue and controls the multiplexer to output the selected ones of the data items by selecting a predetermined number of data items from the queue during an arbitration cycle, the arbitration logic giving higher priority to data items in later stages of the queue.

The Examiner, in rejecting claim 22, contends that Bronson discloses a plurality of queues, but concedes that Bronson does not "teach the use of a multiplexer connected to multiple stages of a queue, outputting selected data items, and coupled to and controlled by the I/O bus control logic 152." (Office Action, paragraph spanning pages 8 and 9). The Examiner, however, contends that this would have been an obvious modification "since multiplexers are shown to be used in the selection of signals (Figure 3, reference #144) and such a component would be useful in selecting signals from either bus 149 or bus 151 (Figure 3)." (Office Action, page 9).

Applicants submit that the Examiner has not made a *prima facie* case of obviousness under § 103. Although Bronson discloses a multiplexer 144, multiplexer 144 is not configured like the multiplexer recited in claim 22. In stark contrast, multiplexer 144 is explicitly shown as connecting only to the input of command queue 146. Bronson is completely devoid of any disclosure or suggestion to modify the multiplexer of Bronson as suggested by the Examiner. The fact that a multiplexer can be used to "select signals" in no way discloses or suggests the multiplexer of claim 22, which "has a plurality of inputs connected to different stages of the queue." Applicants submit that the Examiner, in making the rejection of claim 22, is impermissibly using hindsight gleaned from Applicants' specification.

The Examiner additionally points to column 8, lines 42-55 of Bronson as "[implying] the need for input arbitration into bus control logic 152." (Office Action, pages 3 and 9). This section of Bronson states:

> INR and IRR commands leaving the interrupt router on line 137 are delivered to high priority I/O command queue 150. The commands in this queue 150 are considered separately from the normal priority command queue 148 for output onto the I/O bus 102. If the normal priority command queue 148 is stalled because of busy conditions at an I/O destination, high priority queue 150 is still serviced and commands can continue to be drained out onto I/O bus 102. This implementation effectively allows INR and IRR commands to pass MMIO accesses and eliminates the deadlocks that can arise when I/O devices have MMIO queue full conditions pending the re-enabling of interrupt processing (waiting for INR or IRR).

This section of Bronson relates to the operation of high priority output queue 150 relative to the operation of normal priority output queue 148. Because queues 148 and 150 of Bronson are two different queues, INR and IRR commands in

high priority queue 150 can continue to be output even when queue 148 has a "queue full condition." Applicants submit that multiple, different priority queues, as disclosed by Bronson, in no way suggest the features of claim 22, such as the multiplexer that has "a plurality of inputs connected to different stages of the queue, the multiplexer outputting selected ones of the data items read from the queue." Having multiple queues of different priority do not, as the Examiner states, "imply the need for input arbitration," much less suggest the multiplexer configured as is recited in claim 22.

Although the Examiner includes Umeki in the initial statement of the rejection of claim 22, the Examiner does not reference Umeki when discussing the rejection of claim 22. Accordingly, it appears to Applicants that the Examiner does not intend to include Umeki in the rejection of claim 22. In any event, Applicants submit that Umeki does not cure the above noted deficiencies of Bronson.

For at least these reasons, Applicants submit that the rejection of claim 22 under § 103 is improper and should be withdrawn. The rejections of claims 23-25, at least by virtue of their dependency on claim 22, are also improper and should be withdrawn.

Rejection of Claims 14-19
Based on Parks, Bronson and Umeki

Claim 14 is directed to a network device including, among other things, a request manager configured to receive memory requests, a plurality of parallel processors configured to receive the memory requests from the request

manager, and a memory request arbiter configured to receive the memory requests from the plurality of processors. The Examiner contends that Parks discloses the request manager, the plurality of parallel processors, and a memory request arbiter, although the Examiner concedes that Parks does not disclose or suggest the details of the memory request arbiter recited in claim 14. (Office Action, page 4). The Examiner relies on Bronson and Umeki to disclose these features.

Parks is directed to a system for connecting a plurality of I/O channels to a single computer system bus. (Parks, Title and Abstract). Parks uses a system controller 20 to connect a system bus 14 to I/O channels 10 and 12. (Parks, Fig. 1 and column 3, lines 47-57).

Contrary to the Examiner's assertions, the Applicants submit that Parks does not disclose or suggest, as is recited in claim 14, "a plurality of parallel processors configured to receive the memory requests from the request manager." Although Parks discloses two processors 16 and 18, these processors appear to be standard processors in a personal computer system. (see Parks, column 4, lines 10-18). Processors 16 and 18 of Parks, however, are not disclosed or suggested as being configured to receive memory requests from a request manager. The Examiner contends that system controller 20 corresponds to the request manager recited in claim 14. Controller 20 is described by Parks as controlling "the prioritization and input of data from the two EISA I/O channels 10, 12." (Parks, column 3, lines 55-57). One of ordinary skill in the art will recognize that an EISA bus controller in no way discloses or

suggests a request manager that is configured to receive memory requests and transmit the memory requests to processors. Accordingly, Applicants submit that Parks does not disclose or suggest a request manager, as recited in claim 14.

The memory request arbiter of claim 14 is further recited as including: an input port connected to receive the memory requests from the plurality of processors, a queue corresponding to each of the plurality of parallel processors, each of the queues configured to enqueue and dequeue memory requests of the corresponding parallel processor, and a buffer configured to receive memory requests dequeued from the queues when the queues contain memory requests and to receive memory requests directly from the input port when the queues do not contain memory requests. The Examiner contends that Bronson and Umeki disclose these features and that one of ordinary skill in the art would be motivated to modify Parks to include the features of Bronson and Umeki. Applicants respectfully disagree.

For example, neither Bronson nor Umeki discloses or suggests "a queue corresponding to each of the plurality of parallel processors, each of the queues configured to enqueue and dequeue memory requests of the corresponding parallel processor." Although Parks discloses multiple processors, the processors of Parks, as discussed above, are not configured to receive memory requests from a request manager. Bronson and Umeki completely fail to disclose or suggest a plurality of parallel processors, and could therefore not possibly disclose queues corresponding to a plurality of processors. Accordingly, one of ordinary skill in the art would not be motivated to combine Parks, Bronson,

and Umeki to obtain "a queue corresponding to each of the plurality of parallel processors, each of the queues configured to enqueue and dequeue memory requests of the corresponding parallel processor," as recited in claim 14.

For at least these reasons, Applicants submit that the rejection of claim 14 based on Parks, Bronson, and Umeki is improper and should be withdrawn. Claims 15-19 depend from claim 14. At least by virtue of this dependency, Applicants submit that the rejection of these claims is also improper and should be withdrawn.

New Claims 26 and 27

New claims 26 and 27 depend from claims 1 and 8, respectively. Applicants submit that these claims are not disclosed or suggested by the prior art of record and are therefore directed to allowable subject matter.

Conclusion

In view of the foregoing amendments and remarks, Applicants respectfully request the Examiner's reconsideration of this application, and the timely allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 CFR 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

By: 
Brian E. Ledell
Reg. No. 42,784

11240 Waples Mill Road
Suite 300
Fairfax, Virginia 22030
(571) 432-0800
Customer Number: 44987

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